

2403000502049005
EXAMINATION FEBRUARY-MARCH 2024
BACHELOR OF SCIENCE(SECOND SEMESTER) (NEP)
MDC- COMBINATIONAL CIRCUIT DESIGN THEORY
- LEVEL 4

[Time: As Per Schedule]

[Max. Marks: 25]

Instructions:

1. Fill up strictly the following details on your answer book

a. Name of the Examination : **BACHELOR OF SCIENCE (NEP)(SECOND SEMESTER)**

b. Name of the Subject : **MDC- COMBINATIONAL CIRCUIT DESIGN THEORY - LEVEL 4**

c. Subject Code No : **2403000502049005**

2. Sketch neat and labelled diagram wherever necessary.
3. Figures to the right indicate full marks of the question.
4. All questions are compulsory.

Seat No:

--	--	--	--	--	--

Student's Signature

Q.1 One word or short answer (Any 5)

5

- 1) What is meant by don't care condition?
- 2) What do you mean by latch?
- 3) What is race around condition in RS flip flop?
- 4) Draw the diagram of T flip flop
- 5) What do you mean by quad and octet in K map?
- 6) Explain half subtractor using diagram and truth table

Q.2 A. Using K-map design a full adder circuit.

5

B. Minimize the following function with the help of a K-map and realize it using minimum number of gates.

5

$$F = \sum m (1, 3, 5, 7, 9, 12, 13).$$

OR

- Q.2** **A.** Using K-map design a Binary to Gray code converter circuit **5**
- B.** Explain the difference between combinational logic circuits and sequential logic circuits **5**
- Q.3** **A.** What is flip-flop? Explain the basic concept of flip-flop. Design a D flip-flop and explains it's working. **5**
- B.** Explain the operation of clocked RS flip flop using clock diagram. **5**

OR

- Q.3** **A.** Explain the operation of a 3 bit asynchronous down counter with its logic diagram, truth table and waveform. **5**
- B.** Mention the difference between synchronous and asynchronous counters **5**
